

AMENDMENTS TO THE CLAIMS

1. (currently amended) An NROM memory transistor comprising:
 - a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
 - a nanolaminate gate dielectric formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric composed of oxide – nitride – HfO_2 wherein the nitride layer is a homogeneous nitride layer; and
 - a control gate formed on top of the gate dielectric.
- 2 – 34. (Canceled)
35. (Previously Presented) The transistor of claim 1 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.
36. (Previously Presented) The transistor of claim 1 wherein the control gate is a polysilicon material.
37. (Previously Presented) The transistor of claim 1 wherein the substrate is comprised of p-type silicon.
38. (Previously Presented) The transistor of claim 1 wherein the nanolaminate gate dielectric is fabricated using atomic layer deposition.
39. (Previously Presented) The transistor of claim 1 wherein the nanolaminate gate dielectric is fabricated using an evaporation technique.
40. (Previously Presented) The transistor of claim 1 wherein the nanolaminate gate dielectric is fabricated using a combination of an atomic layer deposition and an evaporation technique.
41. (currently amended) A non-volatile memory device comprising:
 - a memory array comprising a plurality of NROM memory transistors, each transistor comprising:

a substrate having a pair of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
a nanolaminate gate dielectric formed over the substrate substantially between the pair of source/drain regions, the gate dielectric composed of oxide – nitride – HfO_2 wherein the nitride layer is a homogeneous nitride layer;
and
a control gate formed over the gate dielectric.

42. (Previously Presented) The memory device of claim 41 wherein the pair of source drain regions are n+ doped regions in a p-type substrate.

43. (Previously Presented) The memory device of claim 41 wherein the substrate is silicon and the control gate is polysilicon.

44. (currently amended) An electronic system comprising:

a processor that generates control signals; and
a memory device with a memory array coupled to the processor, the array comprising a plurality of NROM memory cells, each NROM memory cell comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;
a nanolaminate gate dielectric formed over the substrate substantially between each pair of the plurality of source/drain regions, the gate dielectric composed of oxide – nitride – HfO_2 wherein the nitride layer is a homogeneous nitride layer; and
a control gate formed over the gate dielectric.